

What is claimed is:

1. A method for fabricating a semiconductor device using an ArF exposure light source, comprising the steps
5 of:

forming a conducting layer on a semiconductor substrate;

forming a first hard mask layer, a second hard mask layer and a third hard mask layer on the conducting
10 layer in order;

forming a photoresist pattern on the third hard mask layer using an ArF exposure light source to form a predetermined pattern;

forming a first hard mask pattern by etching the
15 third hard mask layer using the photoresist pattern as an etching mask;

forming a second hard mask pattern by etching the second hard mask layer using the first hard mask pattern as an etching mask;

20 removing the first hard mask pattern; and

etching the first hard mask layer and the conducting layer using the second hard mask pattern as an etching mask and forming a stacked hard mask pattern having the conducting layer and the second and first hard
25 mask patterns.

2. The method in accordance with claim 1, wherein the first hard mask layer is one of a doped polysilicon layer and an undoped polysilicon layer.

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3. The method in accordance with claim 1, wherein the second hard mask layer is one of an oxynitride layer and a silicon nitride layer.

4. The method in accordance with claim 1, wherein the third hard mask layer comprises the same materials as the conducting layer.

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5. The method in accordance with claim 1, wherein the third hard mask layer is etched by an SC-1 ($\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}=1:4:20$) solution.

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6. The method in accordance with claim 1, wherein the first hard mask layer has a thickness in a range of $50\text{\AA} \sim 100\text{\AA}$.

7. The method in accordance with claim 1, wherein the predetermined pattern is one of a gate electrode pattern, a bit line pattern and a metal line pattern.

8. A method for fabricating a semiconductor device using an ArF exposure light source, comprising the steps of:

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forming a conducting layer on a semiconductor substrate;

forming a first hard mask layer, a second hard mask layer and a third hard mask layer on the conducting layer in order;

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forming a photoresist pattern on the third hard mask layer using an ArF exposure light source to form a predetermined pattern;

forming a first hard mask pattern by etching the third hard mask layer using the photoresist pattern as an etching mask;

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etching the second hard mask layer and the first hard mask layer using at least the first hard mask pattern

and forming a triple stacked hard mask pattern having the first hard mask pattern, a second hard mask pattern and a third hard mask pattern; and

5 etching the conducting layer using the triple stacked hard mask pattern as an etching mask and simultaneously removing the first hard mask pattern, to form a stacked structure having the conducting layer, the second hard mask pattern and the third hard mask pattern.

10 9. The method in accordance with claim 8, wherein the first hard mask layer is a LPCVD oxynitride layer and the second layer is a PECVD oxynitride layer.

15 10. The method in accordance with claim 8, wherein the second hard mask layer is at least two times as thick as the first layer.

20 11. The method in accordance with claim 8, wherein the third hard mask layer comprises the same materials as the conducting layer.

25 12. The method in accordance with claim 8, further comprising the step of forming an antireflective coating layer on the third hard mask layer.

13. A method for fabricating a semiconductor device using an ArF exposure light source, comprising the steps of:

30 forming a conducting layer on a semiconductor substrate;

forming a first hard mask layer and a second hard mask layer on the conducting layer in order;

forming a photoresist pattern on the second hard mask layer using an ArF exposure light source to form a predetermined pattern;

forming a first hard mask pattern by etching the
5 second hard mask layer using the photoresist pattern as an etching mask;

etching the first hard mask layer using at least the first hard mask pattern and forming a second hard mask pattern, thereby forming a first resulting structure;

10 depositing an insulation layer on the first resulting structure; and

patterning the conducting layer using the second hard mask pattern as an etching mask.

15 14. The method in accordance with claim 13, wherein the insulation layer is one of a flowable insulation layer and an organic polymer.

15. The method in accordance with claim 13,
20 wherein the first hard mask layer is a nitride layer and the second hard mask layer is a conducting layer which is one of a tungsten layer and a tungsten nitride layer.

16. The method in accordance with claim 15,
25 wherein the flowable insulation layer is one of a SOG layer and an APL layer.

17. The method in accordance with claim 14,
wherein the step of removing the insulation layer and the
30 first hard mask pattern includes the steps of:

applying a first wet etching process using a fluoride solution to remove a portion of the insulation layer;

applying a second wet etching process using an SC-1 solution to remove the first hard mask pattern; and

applying a third wet etching process using the fluoride solution to remove the residual of the first hard mask pattern.

18. The method in accordance with claim 14, further comprising the step of forming an antireflective coating layer on the third hard mask layer.

19. The method in accordance with claim 13, wherein the predetermined pattern is one of a gate electrode pattern, a bit line pattern and a metal line pattern.